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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,433	04/20/2004	Fumitoshi Mizutani	089367-0127	2720

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EXAMINER	
REDDIVALAM, SRINIVASA R	
ART UNIT	PAPER NUMBER
2419	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/827,433	**Applicant(s)** MIZUTANI ET AL.	
	Examiner SRINIVASA R. REDDIVALAM	**Art Unit** 2419	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 05 August 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *3* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-19*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Chirag G Shah/
Supervisory Patent Examiner, Art Unit 2419

/Srinivasa R Reddivalam/
Examiner, Art Unit 2419

Continuation of 11. does NOT place the application in condition for allowance because: In pages 7-8 of Remarks, regarding independent claim 1, Applicants mention that Horvath does not teach or suggest a plurality of reception interface sections that each includes an arithmetic operation unit, an I/0 unit, and a memory bridge that provides data from said arithmetic operation unit to said I/0 unit of the respective reception interface section and further, Horvath does not teach or suggest that an error in the received data is detected by the memory bridge of one of reception interface sections, and that the memory bridge that detected the communication error notifies the memory bridges of the other reception interface sections of the communication error and Applicant's also mention that Meyers does not teach or suggest that a memory bridge of one reception interface section notifies the memory bridges of the other reception interface sections of the communication error.

However, the Examiner respectfully disagrees to these statements from the Applicants as Meyers et al. teach an apparatus wherein upon occurrence of an error in received data by one of reception interface sections, sends a communication error signal to all other of reception interface sections to stop data reception from data sender (see Figs. 1A, 2, 6 and 8 and page 14, lines 1-28 wherein upon encountering an error by one interface unit, that will cause the interface units to diverge and the resulting difference in the selected stage communicated to the compare circuits, will cause the circuits to issue a 'lost sync' error signal which is equivalent to issuing the error signal and also passing of the message packet information by one interface unit to the companion interface unit for cross-checking for errors is mentioned). Meyers et al. also teach each of said reception interface sections includes an arithmetic operation unit , an I/0 unit, and a memory bridge that provides data from said arithmetic operation unit to said I/0 unit of the respective reception interface section (see Figures 1A and 2 wherein Processor_Unit/ arithmetic_operation_unit inside the CPU 12A, blocks 14A/16A & 14B/16B in Fig.1A for an I/O unit and block 24a/b for Interface unit/memory bridge in Fig.2 are shown and also see Fig.1A & Fig.2 and page 10, lines 20-25 wherein block 24a/b i.e. Interface unit/memory bridge providing/handling all I/O traffic/data between CPU 12A and I/O unit is mentioned). Meyers et al. teach (see Figs. 6 and 8 and page 14, lines 1-28) that upon encountering an error by one interface_unit/memory_bridge, issuing the error signal and also mention passing of the message packet information by one interface_unit/memory_bridge to the companion interface_unit/memory_bridge for cross-checking for errors which is equivalent to 'wherein said error in said received data is detected by said memory bridge of said one of said reception interface sections and wherein said memory bridge of said one of said reception interface sections sends the communication error signal to said other memory bridges of said other reception interface sections'. Thus, Horvath in combination with Meyers et al. teach all the limitations of claim1 as mentioned in the previous office action under Claim Rejections.

In page 8 of Applicant's Remarks, Applicants further mention that the reception interface sections 24a, 24b in Meyers correspond to I/O units, and are not units that provide for data transfer between an I/O unit and an arithmetic operation unit. Howevr, the Examiner respectfully disagrees to this statement from the Applicant as reception interface sections 24a, 24b in Meyers correspond to units that provide for data transfer between an I/O unit and an arithmetic operation unit (see Figures 1A and 2 wherein Processor_Unit/ arithmetic_operation_unit inside the CPU 12A, blocks 14A/16A & 14B/16B in Fig.1A for an I/O unit and block 24a/b in Fig.2 for Interface unit/memory bridge are shown and also see Fig.1A & Fig.2 and page 10, lines 20-25 wherein block 24a/b i.e. Interface unit/memory bridge providing/handling all I/O traffic/data between CPU 12A and I/O unit is mentioned).

In page 8 of Remarks, Applicants further mention that in Meyer's reference, state machine clearly does not correspond in any way, shape or form to a memory bridge that provides data from an arithmetic operation unit to an I/O unit of a reception interface unit. However, the Examiner respectfully disagrees to this statement from the Applicant as Meyers et al. teach a memory bridge that provides data from said arithmetic operation unit to said I/0 unit of the respective reception interface section (see Fig.1A and page 10, lines 20-25 wherein block 24a/b i.e. Interface_unit/memory_bridge providing/handling all I/O traffic/data between CPU 12A and I/O unit is mentioned). Meyers et al. also teach that the interface_units 24a/b (or memory bridges) operate in lock step synchronism, checking for errors can be performed by monitoring the operating states of these paired interface units by continuous comparison of certain of their internal states and if an interface unit encounters an error, that activity will cause the interface units to diverge which will result into different states for the state machines (see page 14, lines 1-18).

In page 9 of Applicant's Remarks, regarding claims 17-19, Applicant mentions that nowhere in the portion i.e. in page 19 of Meyers, and nowhere in Figures 5 and 10 of Meyers, is there any teaching of the use of an open-drain signal to send error messages between the memory interfaces 70. However, the Examiner respectfully disagrees to this statement from the Applicant as Meyers et al. teach the data processing apparatus wherein said memory bridge of said one of said reception interface sections sends the communication error signal to said other memory bridges of said other reception interface sections as an open drain signal (see Figures 5 and 10 and page 19, lines 34-58 wherein each memory interface 70a/b of Interface_unit/memory_bridge receiving and comparing data bits and asserting/sending an error_signal/ECC_logic_error_signal/open_drain_signal on detecting error condition that will result in setting the interrupt register state is mentioned and since sending an error signal is done by ECC check circuit/digital_logic_circuit, the error signal can be considered as equivalent to open drain signal.